INTEL® SPECIFICATION ADDENDUM FOR THE JEDEC DDR266 SPECIFICATION

Rev. 1.0 draft a
November 12, 2001

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Revision History

Revision History (starting from Rev 0.7, history reflects changes with respect to the DDR Rev0.9 spec)

Revision Info	Page of Revision	Description of Change
Revision 1.0	18	tXPDN spec changed to 7.5ns for DDR266, consistent with JEDEC spec
Revision 0.9	8	Clarified DLL normal operating mode select
	8	Changed time for DLL enable to any executable command
Revision 0.8	12	Updated Maximum I_{DD7A} Specification
	15,16	Updated I_{DD} description. Replaced 20ns with 2 clocks. Added DDR266 I_{DD7A} pattern diagram
	21	Added Note 35 to table
Revision 0.7	4	Added DDR266 to features
	8	Modified power-up sequencing requirement
	9	Added note for DM capacitance
	13, 14	Added DDR266 Overshoot/Undershoot requirement
	14, 15	Added DDR266 power requirements
	15, 16	Added DDR266, DDR266-A/-B timing specifications
	17, 18,19	Changed AC-AC slew rates to DC-AC slew rates
	21	Added note 35 – Clock slew rate derating table

Objective

This Specification addendum calls out changes to the JEDEC DDR SDRAM specification Rev 0.9 (dated 7/20/99). The intent of this document is to clarify and detail specifications so as to create a more robust, cost effective, and compatible solution for DDR Memory.

Note: Page number references are to the JEDEC DDR SDRAM specification Rev 0.9.

Features (pg. 1)

?? V_{DD} = 2.5V ? 0.2V only
?? DDR 200 Speed Grades:
  ?? DDR200 (t_{CK} ? 10 ns)
?? DDR 266 Speed Grades:
  ?? DDR266B (t_{CK} ? 7.5 ns, CL=2.5, tRCD=3, tRP=3)
  ?? DDR266A (t_{CK} ? 7.5 ns, CL=2, tRCD=3, tRP=3)
  ?? DDR266 (t_{CK} ? 7.5 ns, CL=2, tRCD=2, tRP=2)

General Description (pg. 1)

Supported configurations are given in the table below.

DRAM size	Supported Configurations
64Mb	x4, x8, x16
128Mb	x4, x8, x16
256Mb	x4, x8, x16
512Mb	x4, x8, x16
1Gb	x4, x8, x16

Table of Contents (pg. 2)

Topics in which changes have occurred versus the JEDEC 0.9 DDR Spec.

Pin Assignment Diagram
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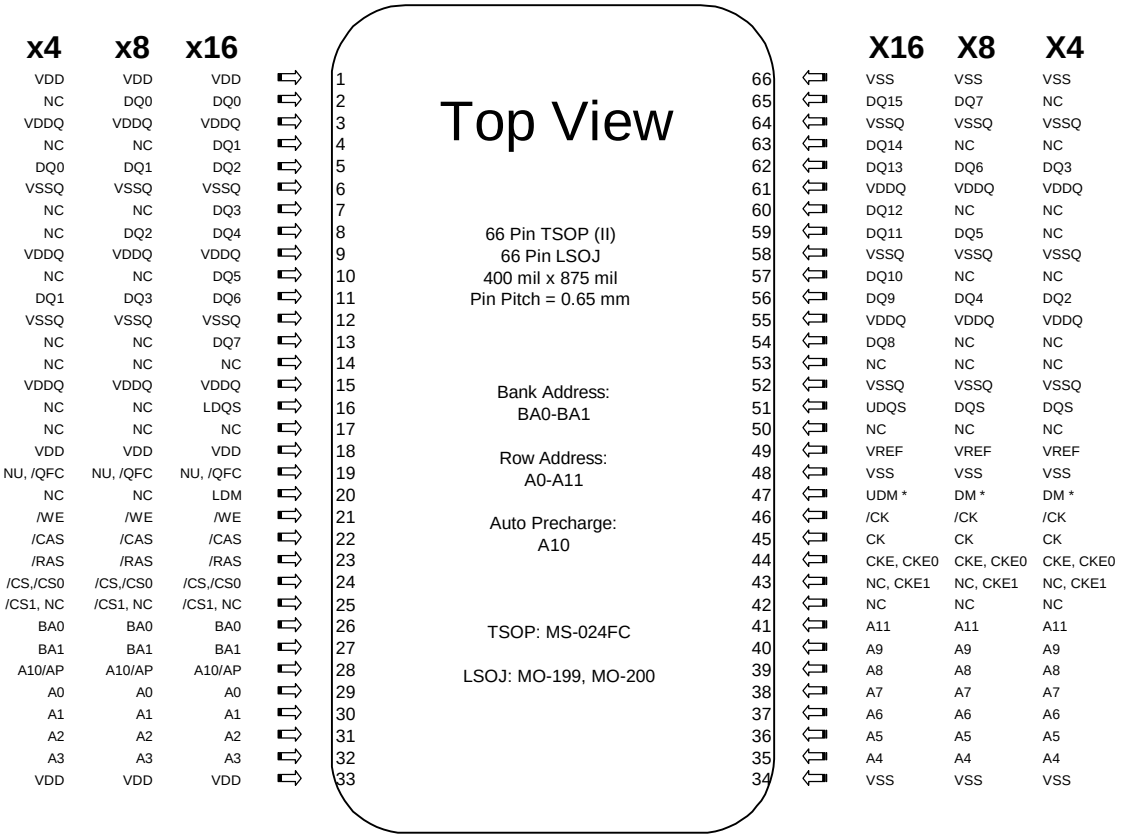
AC Operating Conditions
IDD Specifications and Conditions
Electrical Characteristics and AC Timing for PC266/PC200 – Absolute Specifications
QFC is not required to be supported

Pin Assignment Diagram (pg. 3)

64/128M DDR SDRAM (x4/x8/x16) Pin-out



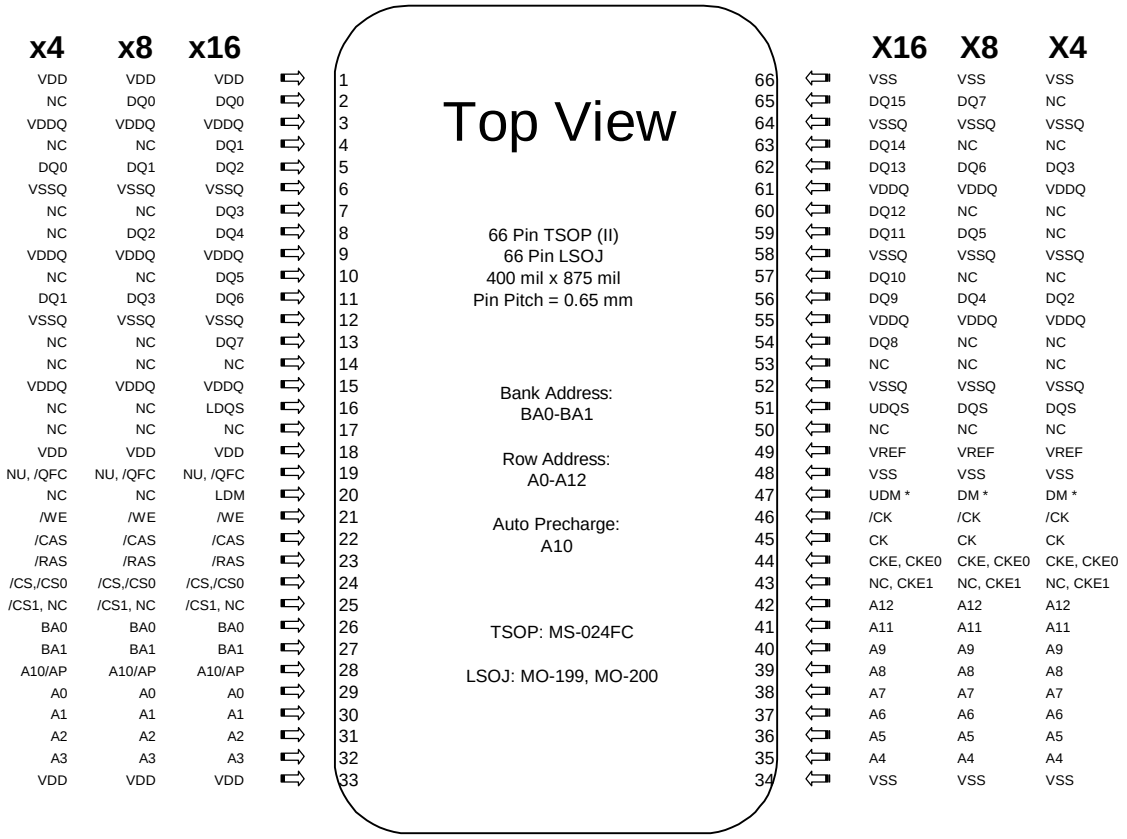
64M Column Address Table

Organization	Column Address
16M x4	A0-A9
8M x8	A0-A8
4M x16	A0-A7

128M Column Address Table

Organization	Column Address
32M x4	A0-A9, A11
16M x8	A0-A9
8M x16	A0-A8

256/512M DDR SDRAM (x4/x8/x16) Pin-out



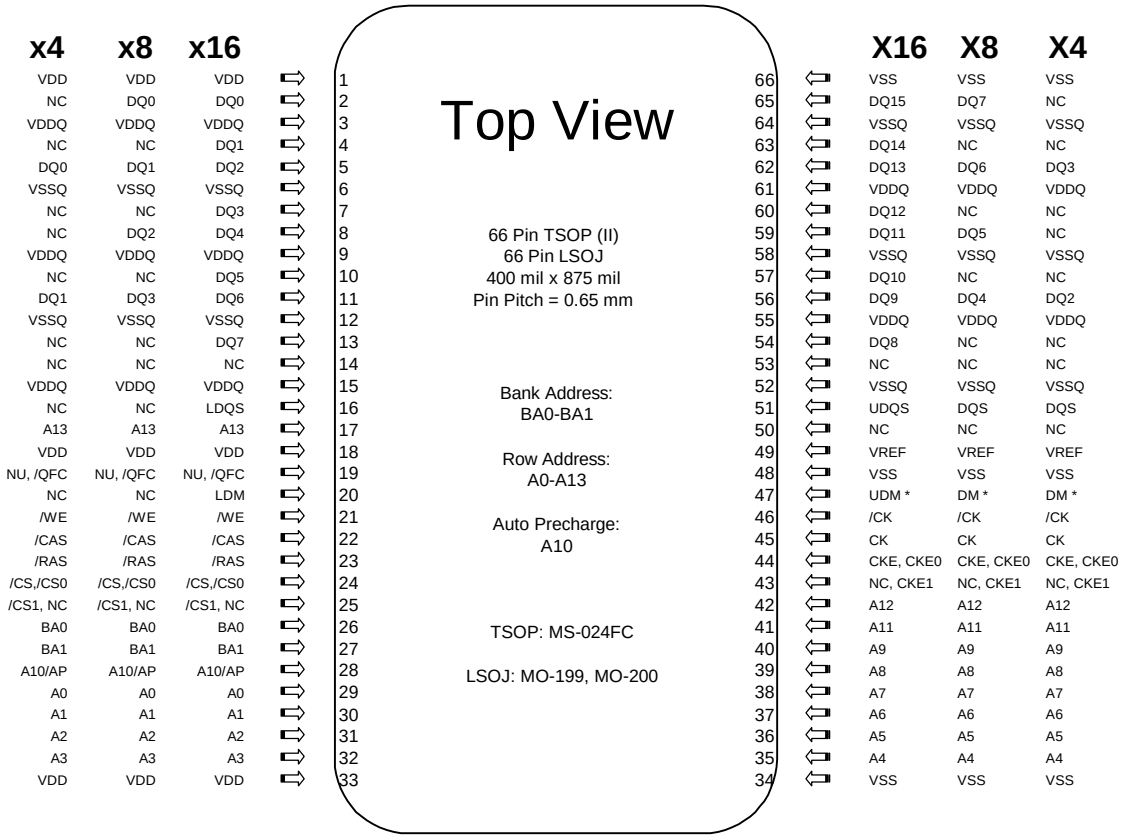
256M Column Address Table

Organization	Column Address
64M x4	A0-A9, A11
32M x8	A0-A9
16M x16	A0-A8

512M Column Address Table

Organization	Column Address
128M x4	A0-A9, A11, A12
64M x8	A0-A9, A11
32M x16	A0-A9

1G DDR SDRAM (x4/x8/x16) Pin-out



1G Column Address Table

Organization	Column Address
256M x4	A0-A9, A11, A12
128M x8	A0-A9, A11
64M x16	A0-A9

Functional Block Diagrams (pg. 4, 5, 6)

Note 3: Diagrams in JEDEC Spec (pgs. 4, 5 and 6) represent the 64Mb configuration only. Other functional diagrams for 128, 256, 512 Mb and 1 Gb have not been included but would follow the same format.

Pin Descriptions (pg. 7)

In order to accommodate 128Mb and higher devices, pins A12 and A13 must be assigned and additional functionality must be defined. Pin A12 has been assigned to Pin 42. Pin A13 has been assigned to Pin 17 for 1 Gb parts only. Additional Row and Column addresses for 128, 256, 512 Mb and 1 Gb devices have been defined. The table below describes the changes.

Parameter	Target
Pin 42	64, 128 Mb: NC 256, 512 Mb, 1 Gb: A12
Pin 17	64 Mb to 512 Mb: NC 1 Gb: A13
Addresses	64, 128 Mb: A(11:0) 256, 512 Mb: A(12:0) 1 Gb: A(13:0)

Internally all VSS , VSSQ, VDD, and VDDQ pins must be connected up to the die, unless otherwise noted in the vendor's data sheet or validation documentation. Externally all power and ground pins must be connected to the appropriate power and ground networks. This insures minimum impact to output slew rates and input noise. DM may be driven high, low or floated during reads.

Functional Description (pg. 8)

DQ, DQS and DM signals may be floated to V_{TT} when no data is being transferred.

Initialization (pg. 8)

Delete the following three sentences from the Initialization paragraph:

"~~Power must first be applied to V_{DD}, then to $V_{DD}Q$, and finally to V_{REF} (and to the system V_{TT}). V_{TT} must be applied after $V_{DD}Q$ to avoid device latch-up, which may cause permanent damage to the device. V_{REF} can be applied any time after $V_{DD}Q$, but is expected to be nominally coincident with V_{TT}.~~"

and replace with :

No power sequencing is specified during power up or power down given the following criteria:

- V_{DD} and $V_{DD}Q$ are driven from a single power converter output, and
- V_{TT} is limited to 1.44V (reflecting $V_{DD}Q$(max)/2 + 50mV V_{REF} variation + 40mV V_{TT} variation), and
- $V_{REF} < V_{DD}Q + 0.3V$, and
- A minimum resistance of 42 ohms (22 ohm series resistor + 22 ohm parallel resistor – 5% tolerance) limits the input current from the V_{TT} supply into any pin.

If the above criteria cannot be met by the system design, then the following table must be adhered to during power up:

Voltage Description	Sequencing	Voltage Relationship to avoid latch-up
$V_{DD}Q$	After or with V_{DD}	$< V_{DD} + 0.3V$
V_{TT}	After or with $V_{DD}Q$	$< V_{DD}Q + 0.3V$
V_{REF}	After or with $V_{DD}Q$	$< V_{DD}Q + 0.3V$

Operating Mode (pg. 10)

Change the last sentence of the first paragraph

From:

A Mode Register Set command issued to reset the DLL should always be followed by a Mode Register Set command to select the normal operating mode.

To:
A Mode Register Set command issued to reset the DLL should always be followed by a Mode Register Set command to select the normal operating mode (i.e. with A8=0).

DLL Enable/Disable (pg. 12)

The last sentence should be changed as follows -
From:
Any time the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.
To:
Any time the DLL is enabled, 200 clock cycles must occur before any executable command can be issued.

Truth Table 4 – Current State Bank n – Command to Bank M (Notes) (pg. 52)

Modify note "3" to add an optional feature called "concurrent auto-precharge":

Read with Auto
Precharge Enabled: See following text, notes 3a, 3b and 3c:

Write with Auto
Precharge Enabled: See following text, notes 3a, 3b and 3c:

3a. For devices which do not support the optional "concurrent auto precharge" feature, the read with auto precharge enabled ….. *(rest of note 3a is unchanged)*

3b. For devices which do support the optional "concurrent auto precharge" feature, a read with auto precharge enabled, or a write with auto precharge enabled, may be followed by any command to the other banks, as long as that command does not interrupt the read or write data transfer, and all other related limitations apply (e.g. contention between READ data and WRITE data must be avoided.)

3c. The minimum delay from a read or write command with auto precharge enabled, to a command to a different bank, is summarized below, for both cases of "concurrent auto precharge" supported or not:

From command	To command (different bank, non-interrupting command)	Minimum delay, without concurrent AP support	Minimum delay, with concurrent AP support	Units
Write w/AP	Read or Read w/AP	1 + (BL/2) + (tWR/tCK) (rounded up)	1 + (BL/2) + tWTR	tCK
	Write or Write w/AP	1 + (BL/2) + (tWR/tCK) (rounded up)	BL/2	tCK
	Precharge or Activate	1		tCK
Read w/AP	Read or Read w/AP	BL/2		tCK
	Write or Write w/AP	CL(rounded up) + (BL/2)		tCK
	Precharge or Activate	1		tCK

Capacitance (pg. 54)

Parameter	Symbol	MIN	MAX	UNITS	NOTES
Input Capacitance: (CK, /CK)	C_{I1}	2.0	3.0	pF	Note 13
Input Capacitance: Input only pins (including CKE but not including CK, /CK)	C_{I2}	2.0	3.0	pF	Note 13
Input/Output Capacitance: DQ, DQS, DM	C_{IO}	4.0	5.0	pF	Note 13
Delta I/O Capacitance: DQ, DQS, DM	C_{IOD}	NA	0.5	pF	Note 13
Delta Input Capacitance: (CK, /CK only)	C_{ID}	NA	0.25	pF	Note 13

Note: I/O capacitance for DM applies to x8 and x16 parts only. Delta capacitance for DQ, DQS and DM only includes DM for x8 and x16 parts. DM does not have to be measured for x4 parts, since it is tied to ground in all DIMM applications.

In addition to verifying the above values at 100MHz, the S11 data will be measured and, using the procedure developed by Intel, the resulting fit values will be compared to the min and max values provided.

Address and Command S11 Parametric Fit (new)

Parameter	Symbol	MIN	MAX	Units	Notes
Fit Inductance	L_{AC}	2.0	8.0	nH	
Fit Capacitance	C_{AC}	2.0	3.0	pF	
Fit Resistance	R_{AC}	8.0	32.0	Ohms	

DQ and DQS S11 Parametric Fit (new)

Parameter	Symbol	MIN	MAX	Units	Notes
Fit Inductance	L_{DQ}	2.0	7.0	nH	
Fit Capacitance	C_{DQ}	4.0	5.0	pF	
Fit Resistance	R_{DQ}	5.0	20.0	Ohms	

CK and /CK S11 Parametric Fit (new)

Parameter	Symbol	MIN	MAX	Units	Notes
Fit Inductance	L_{CK}	2.0	9.0	nH	
Fit Capacitance	C_{CK}	2.0	3.0	pF	
Fit Resistance	R_{CK}	8.0	40.0	Ohms	

DM S11 Parametric Fit (new)

Parameter	Symbol	MIN	MAX	Units	Notes
Fit Inductance	L_{DM}	2.0	8.0	nH	
Fit Capacitance	C_{DM}	4.0	5.0	pF	
Fit Resistance	R_{DM}	5.0	40.0	Ohms	

Electrical Characteristics and DC Operating Conditions (pg. 54)

Parameter	Symbol	MIN	MAX	UNITS	NOTES

Supply Voltage	V_{DD}	2.3	2.7	V	
I/O Reference Voltage	V_{REF}	$V_{DD}Q/2$ - 50mV	$V_{DD}Q/2$ + 50mV	V	Note 6 (pg 60) (modified)
Input High (Logic1) Voltage	$V_{IH(DC)}$	V_{REF} +0.15	V_{DD} +0.3	V	Note 32 (new)
Input Low (Logic 0) Voltage	$V_{IL(DC)}$	-0.3	V_{REF} -0.15	V	Note 32 (new)
Input Leakage Current (All other pins not under test = 0V) Any input $0V < V_{IN} < V_{DD}$	I_I	-2	2	?A	
V/I Matching: Pullup current to Pulldown current ratio		.71	1.4	None	V/I Requirement 9 (pg 55) (new)

IV Curve Requirements (pg. 55):

2) The variation in the driver pulldown current **at nominal temperature and voltage** is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure a as shown on pg. 55 of the JEDEC spec rev 0.9.

4) The variation in the driver pullup current **at nominal temperature and voltage** is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure b as shown on pg. 55 of the JEDEC spec rev 0.9.

5) Delete this requirement

6) Delete this requirement

7) These characteristics obey the SSTL-2 class II standards.

8) This specification is intended for DDR SDRAM only.

9) The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages from 0.25V to 1.0V. For example, the pulldown current at 0.5V should match the pullup current at ($V_{DD}Q$-0.5V). The ratio represents the maximum process variation between either the DQS pullup and its associated DQ pulldowns, or the DQS pulldown and its associated DQ pullups.

Normal Output Drive Characteristics (pg. 56)

Voltage (V)	Pull-Down Current (mA)				Pull-Up Current (mA)			
	Nominal Low	Nominal High	Minimum	Maximum	Nominal Low	Nominal High	Minimum	Maximum
0.1	6.0	6.8	4.6	9.6	-6.1	-7.6	-4.6	-10.0
0.2	12.2	13.5	9.2	18.2	-12.2	-14.5	-9.2	-20.0
0.3	18.1	20.1	13.8	26.0	-18.1	-21.2	-13.8	-29.8
0.4	24.1	26.6	18.4	33.9	-24.0	-27.7	-18.4	-38.8
0.5	29.8	33.0	23.0	41.8	-29.8	-34.1	-23.0	-46.8
0.6	34.6	39.1	27.7	49.4	-34.3	-40.5	-27.7	-54.4
0.7	39.4	44.2	32.2	56.8	-38.1	-46.9	-32.2	-61.8
0.8	43.7	49.8	36.8	63.2	-41.1	-53.1	-36.0	-69.5
0.9	47.5	55.2	39.6	69.9	-43.8	-59.4	-38.2	-77.3
1.0	51.3	60.3	42.6	76.3	-46.0	-65.5	-38.7	-85.2
1.1	54.1	65.2	44.8	82.5	-47.8	-71.6	-39.0	-93.0
1.2	56.2	69.9	46.2	88.3	-49.2	-77.6	-39.2	-100.6

1.3	57.9	74.2	47.1	93.8	-50.0	-83.6	-39.4	-108.1
1.4	59.3	78.4	47.4	99.1	-50.5	-89.7	-39.6	-115.5
1.5	60.1	82.3	47.7	103.8	-50.7	-95.5	-39.9	-123.0
1.6	60.5	85.9	48.0	108.4	-51.0	-101.3	-40.1	-130.4
1.7	61.0	89.1	48.4	112.1	-51.1	-107.1	-40.2	-136.7
1.8	61.5	92.2	48.9	115.9	-51.3	-112.4	-40.3	-144.2
1.9	62.0	95.3	49.1	119.6	-51.5	-118.7	-40.4	-150.5
2.0	62.5	97.2	49.4	123.3	-51.6	-124.0	-40.5	-156.9
2.1	62.9	99.1	49.6	126.5	-51.8	-129.3	-40.6	-163.2
2.2	63.3	100.9	49.8	129.5	-52.0	-134.6	-40.7	-169.6
2.3	63.8	101.9	49.9	132.4	-52.2	-139.9	-40.8	-176.0
2.4	64.1	102.8	50.0	135.0	-52.3	-145.2	-40.9	-181.3
2.5	64.6	103.8	50.2	137.3	-52.5	-150.5	-41.0	-187.6
2.6	64.8	104.6	50.4	139.2	-52.7	155.3	-41.1	-192.9
2.7	65.0	105.4	50.5	140.8	-52.8	160.1	-41.2	-198.2

Evaluation Conditions:

Typical	T_J ~ 45?C, $V_{DD}Q$ = 2.5V, typical process
Minimum	T_J ~ 95?C, $V_{DD}Q$ = 2.3V, slow-slow process
Maximum	T_J ~ 5?C, $V_{DD}Q$ = 2.7V, fast-fast process

Temperature (new)

Component vendors shall guarantee proper component operation at T_J up to and including 95?C. For low power parts (IDD7A max specification ? 225mA), the following table will be used to determine the test junction temperature.

Maximum I_{DD7A} Specification	Test Junction Temperature (T_J)
? 425mA	~95?
? 225mA	~87?
? 150mA	~80?

AC Operating Conditions (pg. 57)

Parameter	Symbol	MIN	MAX	UNITS	NOTES
Input High (Logic1) Voltage, for all input and I/O signals	$V_{IH(AC)}$	V_{REF} +0.31		V	Note 32 (new)
Input Low (Logic 0) Voltage, for all input and I/O signals	$V_{IL(AC)}$		V_{REF} -0.31	V	Note 32 (new)

Clamping Specification (new)

Power and ground clamps are required on the following pins –

1. BA0-BA1
2. A0-A13
3. /RAS
4. /CAS
5. /WE

Power & Ground Clamp V-I Characteristics (new)

V-I Characteristics for pins with clamps

Voltage across clamp (V)	Minimum Power Clamp Current (mA)	Minimum Ground Clamp Current (mA)
0.0	0	0
0.1	0	0
0.2	0	0
0.3	0	0
0.4	0	0
0.5	0	0
0.6	0	0
0.7	0	0.05
0.8	0	0.6
0.9	0	1.8
1.0	0.23	3.4
1.2	1.34	7.6
1.4	3.02	13.0
1.6	5.06	18.0
1.8	7.35	25.0
2.0	9.83	31.0
2.2	12.48	38.0
2.4	15.3	46.0

AC Overshoot/Undershoot Specification (new)

Overshoot/Undershoot specification for CS, CKE, BA0-BA1, A0-A13, /RAS, /CAS & /WE pins

Parameter	DDR266 Specification	Notes
Maximum peak amplitude allowed for overshoot	1.5 V	
Maximum peak amplitude allowed for undershoot	1.5 V	
Duration of pulse	? 2.5 ns	
Overshoot/Undershoot area	? 1.875 V-ns	

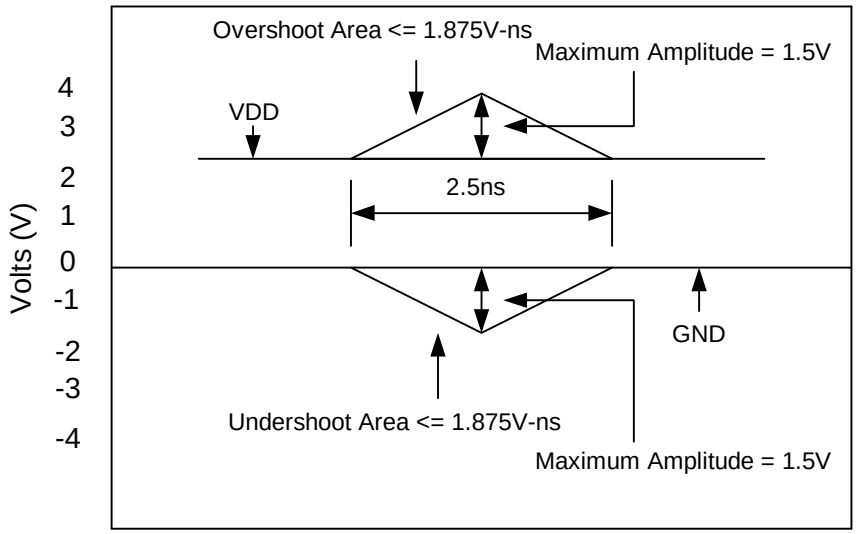


FiG 1 (new): Overshoot/Undershoot Spec for CS, CKE, BA0-BA1, A0-A13, /RAS, /CAS & /WE pins

Overshoot/Undershoot specification for CK, /CK, DQ, DQS & DM pins

Parameter	DDR 266 Specification	Notes
Maximum peak amplitude allowed for overshoot	1.2 V	
Maximum peak amplitude allowed for undershoot	1.2 V	
Duration of pulse	? 1.25 ns	
Overshoot/Undershoot area	? 0.75V-ns	

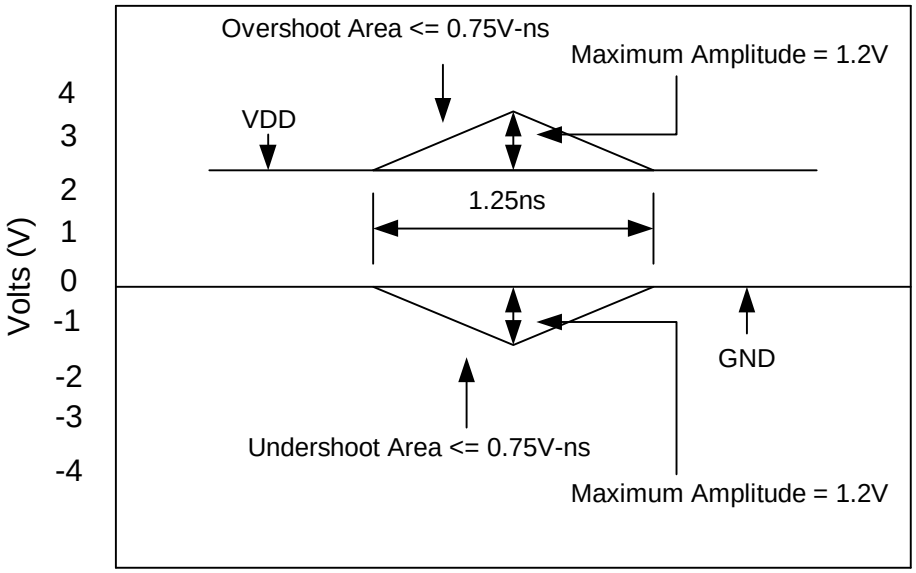


FiG 2 (new): Overshoot/Undershoot Spec for CK, /CK, DQ, DQS & DM pins

I_{DD} Specifications and Conditions (pg. 57)

Parameter	Symbol	MAX (t_{CK} = 7.5 ns, t_{RC} = 67.5 ns)	MAX (t_{CK} = 10 ns)	UNITS	NOTES
IDLE FLOATING STANDBY CURRENT: /CS ? Vih(min); All banks idle; CKE ? Vih (min); Addresses and other control inputs changing once per clock cycle, Vin = Vref for DQ, DQS and DM	I_{DD2F}	? 40 mA for x4 parts	? 35 mA for x4 parts	mA	
IDLE STANDBY CURRENT: … ; **Vin** ? **Vih (min) or Vin** ? **Vil (max) for DQ, DQS and DM**	I_{DD2N}	V/DS*	V/DS*	mA	
PRECHARGE POWER-DOWN STANDBY CURRENT: … ; **Vin = Vref for DQ, DQS and DM**	I_{DD2P}	V/DS*	V/DS*	mA	
IDLE QUIET STANDBY CURRENT: /CS ? Vih(min); All banks idle; CKE ? Vih (min); Addresses and other control inputs stable, Vin = Vref for DQ, DQS and DM	I_{DD2Q}	V/DS*	V/DS*	mA	
ACTIVE STANDBY CURRENT – ALL BANKS ACTIVE: Four banks active; active – precharge; tRC=tRASmax; tCK = 100Mhz; DQ, DQS and DM inputs changing twice per clock cycle; address and other control inputs changing once	$I_{DD3N\ A}$	V/DS*	V/DS*	mA	For Intel test purposes only

per clock cycle					
RANDOM READ CURRENT: 4 banks active read with activate every 2 clocks, AP (Auto Precharge) read every 2 clocks, BL = 4, t_{RCD} = 3, I_{OUT} = 0 mA, 50% DQ, DM and DQS inputs changing twice per clock cycle; 50% addresses changing once per clock cycle	I_{DD7}	V/DS*	V/DS*	mA	*Figure 49 (new) below*
RANDOM READ CURRENT: 4 banks active read with activate every 2 clocks, AP (Auto Precharge) read every 2 clocks, BL = 4, t_{RCD} = 3, I_{OUT} = 0 mA, 100% DQ, DM and DQS inputs changing twice per clock cycle; 100% addresses changing once per clock cycle	I_{DD7A}	? 375 mA for x4 parts up to 256Mb, ? 425 mA for x4 parts, 512Mb	? 325 mA for x4 parts up to 256Mb, ? 375 mA for x4 parts, 512Mb	mA	*Figure 49 (new) below*

V/DS * = Vendor/Device Specific

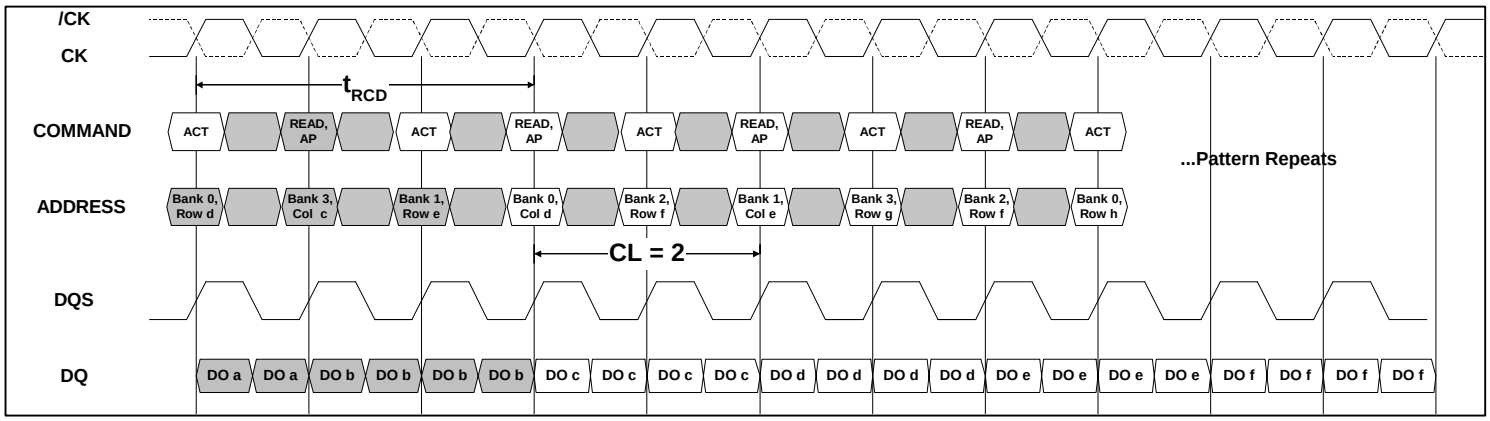


Figure 49a
DDR200 RANDOM READ CURRENT (I_{DD7A}): 4 banks active read with activate every 2 clocks

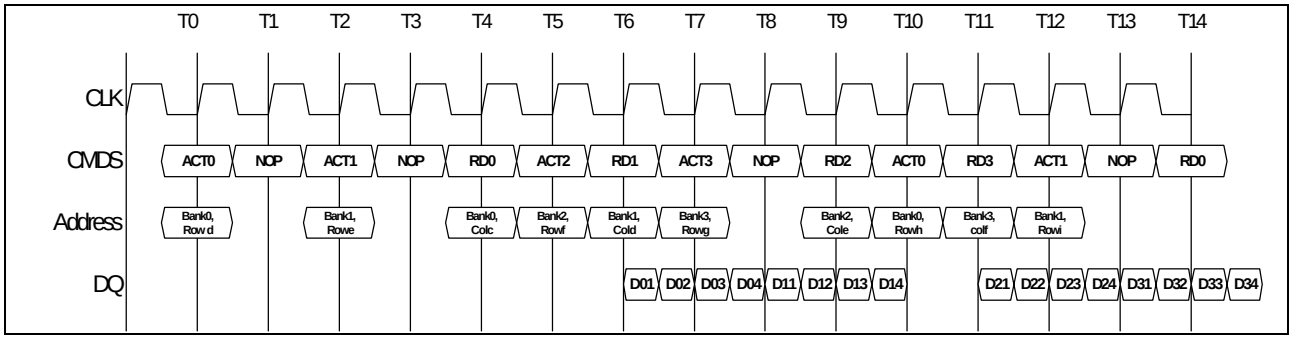


Figure 49b
DDR266 RANDOM READ CURRENT (I_{DD7A}): 4 banks active read with activate every 2 clocks

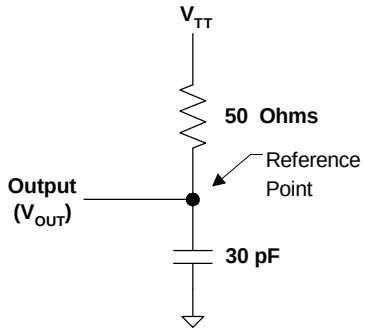
Electrical Characteristics and AC Timing for DDR266/DDR200- Absolute Specifications (pg. 58)

AC Characteristic		DDR 266 (2-2-2)		DDR 266-B DDR 266-A		DDR 200-10 (t_{CK} ? 10 ns)			
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
RAS to READ or WRITE command	t_{RCD}	15		20		20		ns	
RAS precharge	t_{RP}	15		20		20		ns	
RAS cycle time	t_{RC}	60		67.5		70		ns	
Average Periodic Refresh Interval 64, 128 Mb	t_{REFI}		15.6		15.6		15.6	?s	
Average Periodic Refresh Interval 256, 512 Mb, 1Gb	t_{REFI}		7.8		7.8		7.8	?s	
Auto Refresh to Active/Auto Refresh command period for 64, 128, 256, 512 Mb	t_{RFC}	75		75		80		ns	
Auto Refresh to Active/Auto Refresh command period for 1Gb	t_{RFC}	120		120		140		ns	
CK low-level width	t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	Note 31 (new)
CK high-level width	t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	Note 31 (new)
Input Slew Rate (for input only pins)	$t_{SL(I)}$	0.5		0.5		0.5		V/ns	Note 25
Input Slew Rate (for I/O pins)	$t_{SL(IO)}$	0.5		0.5		0.5		V/ns	Note 26, 29 (new)
Output Slew Rate (x4, x8)	$t_{SL(O)}$	1.0	4.5	1.0	4.5	1.0	4.5	V/ns	Note 30 (new)
Output Slew Rate (x16)	$t_{SL(O)}$	0.7	5.0	0.7	5.0	0.7	5.0	V/ns	Note 30 (new)
Output Slew Rate Matching Ratio (rise to fall)	t_{SLMR}	0.67	1.5	0.67	1.5	0.67	1.5		Note 24 (new)
RAS to READ (with AUTO PRECHARGE) for devices not supporting t_{RAS} lockout	t_{RAP}	45 – BL* t_{CK}/2		45 – BL* t_{CK}/2		50 – BL* t_{CK}/2		ns	AP ? t_{RAS} min
RAS to READ (with AUTO PRECHARGE) for devices supporting t_{RAS} lockout	t_{RAP}	15		20		20		ns	t_{RCD} min
Address and Control input hold time	t_{IH}	0.9		0.9		1.1		ns	At input slew rate ? 0.5 V/ns. Note 25, 35 (new).
Address and Control input setup time	t_{IS}	0.9		0.9		1.1		ns	At input slew rate ? 0.5 V/ns. Note 25, 35 (new).
Write Command to first DQS latching transition	t_{DQSS}	0.72	1.28	0.72	1.28	0.75	1.25	t_{CK}	
DQ and DM input hold time	t_{DH}	0.5		0.5		0.6		ns	At input slew rate ? 0.5 V/ns. Notes 26, 27, 28 (new).
DQ and DM input setup time	t_{DS}	0.5		0.5		0.6		ns	At input slew rate ? 0.5 V/ns. Notes 26, 27, 28 (new).
DQS-DQ Skew (for DQS and associated DQ signals) Skew from DQS to last DQ(7:0).	t_{DQSQ}	NA	0.5	NA	0.5	NA	0.6	ns	No minimum specified. Note 31 (new)
Half Period = minimum of actual (t_{CH}, t_{CL})	t_{HP}	45% t_{CK}	NA	45% t_{CK}	NA	45% t_{CK}	NA	t_{CK}	Note 31 (new)
Data Hold from DQS to earliest DQ (7:0) next clock edge	t_{QH}	t_{HP} - t_{QHS}	NA	t_{HP} - t_{QHS}	NA	t_{HP} - t_{QHS}	NA	ns	Replaces t_{DV} Note 31 (new)
Data Hold Skew	t_{QHS}	NA	0.75	NA	0.75	NA	1	ns	
Refresh to Refresh Period 64, 128 Mb	t_{RR}		140		140		140	?s	
Refresh to Refresh Period 256, 512 Mb, 1 Gb	t_{RR}		70		70		70	?s	
Power Down Duration (CKE negated) 64, 128 Mb	t_{PDN}		140		140		140	?s	Figure 39a (new)
Power Down Duration (CKE negated) 256, 512 Mb, 1 Gb	t_{PDN}		70		70		70	?s	Figure 39a (new)

AC Characteristic		DDR 266 (2-2-2)		DDR 266-B DDR 266-A		DDR 200-10 (t_{CK} ? 10 ns)			
Power Down Exit *(Note – exit to read, write and activate)*	t_{XPDN}	7.5		7.5		10		Ns	Figure 39a (new)
Clock cycle time	t_{CK}	7.5	12	7.5	12	10	12	ns	
MODE REGISTER SET command cycle time	t_{MRD}	15		15		20		ns	
ACTIVE bank A to ACTIVE bank B command	t_{RRD}	15		15		20		ns	
Data-out high-impedance time from CK/CKN (DQ/DQS)	T_{HZ}	-1.1	+.75	-1.1	+.75	-1.2	+0.8	ns	Note 18, 35 (new)
Data-out low-impedance time from CK/CKN (DQ)	T_{LZ}	-1.1	+.75	-1.1	+.75	-1.2	+0.8	ns	Note 18, 35 (New
Data-out low-impedance time from CK/CKN (DQS)	T_{LZ}	-.75	+.75	-.75	+.75	-1.1	+0.8	ns	Note 18, 35 (new)
Write recovery time	t_{WR}	15		15		20		ns	
Auto Precharge write recovery + precharge time	t_{DAL}	40		40		40		ns	Note 33 (new)
Read Postamble	t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	Note 34 (new)
Read Preamble	t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	Note 34 (new)
Exit SELF REFRESH to non-READ command	t_{XSNR}	200		200		200		t_{CK}	
DQS input low pulse width	t_{DQSL}	0.35		0.35		0.35		t_{CK}	
DQS input high pulse width	t_{DQSH}	0.35		0.35		0.35		t_{CK}	

Notes (pg. 60):

3) Output AC timing parameters are measured with equivalent load:



4) AC timing and IDD tests may use a V_{IL} to V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK, /CK). Parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns between V_{IL}(AC) and V_{IH}(AC) for the I/O and clock pins and 0.5V/ns for all other input only pins.

6) Includes ?25mV margin for DC offset on $V_{REF,}$ and a combined total of ? 50mV margin for all AC noise and DC offset on V_{REF}, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on V_{REF} and internal DRAM noise coupled to V_{REF}, both of which may result in V_{REF} noise. V_{REF} should be de-coupled with an inductance of ? 3nH.

13) This parameter is sampled. $V_{DD}Q = V_{DD}$ = +2.5V ? 0.2V, f = 100MHz, t_A = 25?C, $V_{OUT(DC)}$ = $V_{DD}Q/2$, $V_{OUT(Peak\ to\ Peak)}$ = 0.2V. DM inputs are classified with I/O pins reflecting the fact that they are matched in loading (to facilitate trace matching at the board level).

24) The ratio of the rising slew rate to the falling slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. The ratio represents the maximum process

variation between either the DQS pullup and its associated DQ pulldowns, or the DQS pulldown and its associated DQ pullups.

25) Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate	? t_{IS}	? t_{IH}
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+50	0
0.3	+100	0

Note: This derating table is used to increase t_{IS}/t_{IH} in the case where the input slew-rate is below .5V/ns.
Input S/H slew rate based on the lesser of the DC-AC slew rate and the DC-DC slew rate as represented in Figure 52.

26) I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate	? t_{DS}	? t_{DH}
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+75	+75
0.3	+150	+150

Note: This derating table is used to increase t_{DS}/t_{DH} in the case where the I/O slew-rate is below 0.5V/ns.
I/O S/H slew rate based on the lesser of the DC-AC slew rate and the DC-DC slew rate as represented in Figure 52.
The derating of notes 26, 27 and 28 are additive.

27) I/O Setup/Hold Plateau Derating

I/O Input Level	? t_{DS}	? t_{DH}
(mV)	(ps)	(ps)
? 280	+50	+50

Note: This derating table is used to increase t_{DS}/t_{DH} in the case where the input level is flat below V_{REF} ?310mV for a duration of up to 2ns. In such instances, Figure 52 should be modified to reflect V_{REF} ? 0.28 instead of V_{REF} ? 0.31.
The derating of notes 26, 27 and 28 are additive.

28) I/O Setup/Hold Delta Inverse Slew Rate Derating

$\frac{1}{SlewRate1} ? \frac{1}{SlewRate2}$	? t_{DS}	? t_{DH}
(ns/V)	(ps)	(ps)
0	0	0
? 0.25	+50	+50
? 0.5	+100	+100

Note: This derating table is used to increase t_{DS}/t_{DH} in the case where the DQ and DQS slew rates differ.
The Delta Inverse Slew Rate is calculated as $\frac{1}{SlewRate1} ? \frac{1}{SlewRate2}$. For example, if slew rate 1 =.5V/ns and slew rate 2=.4V/ns then the Delta Inverse Slew Rate = -0.5ns/V.

Slew rates based on the lesser of the DC-AC slew rate and the DC-DC slew rate as represented in Figure 52.
Input S/H slew rate based on larger of DC-AC delta rise/fall rate and DC-DC delta rise/fall rate.
The derating of notes 26, 27 and 28 are additive.

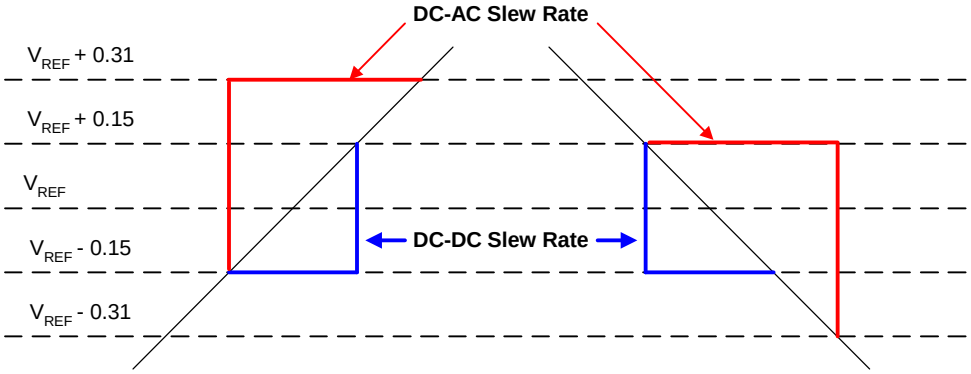


Figure 52: Slew Rate calculation points for comparing DC-AC slew rate and DC-DC slew rate.

29) DQ, DM, and DQS input slew rate specified to prevent double clocking data and preserve setup and hold. Signal through DC region must be monotonic with a rise/fall time ? 1ns measured across V_{REF} ? 150mV.

30) Output slew rate represents the maximum process variation between either the DQS pullup and its associated DQ pulldowns, or the DQS pulldown and its associated DQ pullups. The output slew rate conditions are to be met for any data pattern including all output pins switching at once in the same direction and only one output pin switching. Pullup slew rate is simulated between (V_{TT} - 320mV) ? 250mV under the test condition as shown in Figure 50 (new). Pulldown slew rate is simulated between (V_{TT} + 320mV) ? 250mV under the test condition as shown in Figure 51 (new).

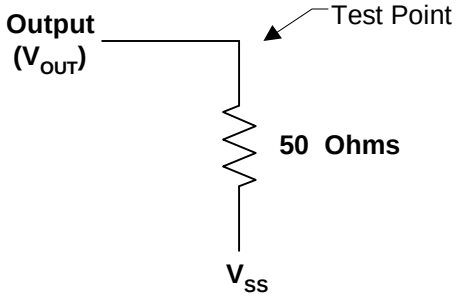


Figure 50: Pullup slew rate test load

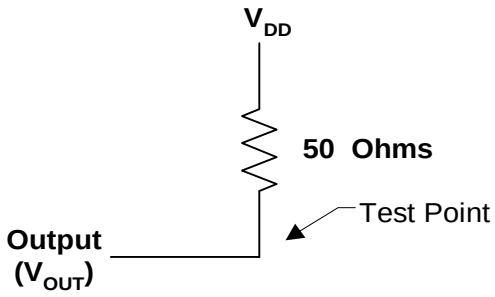
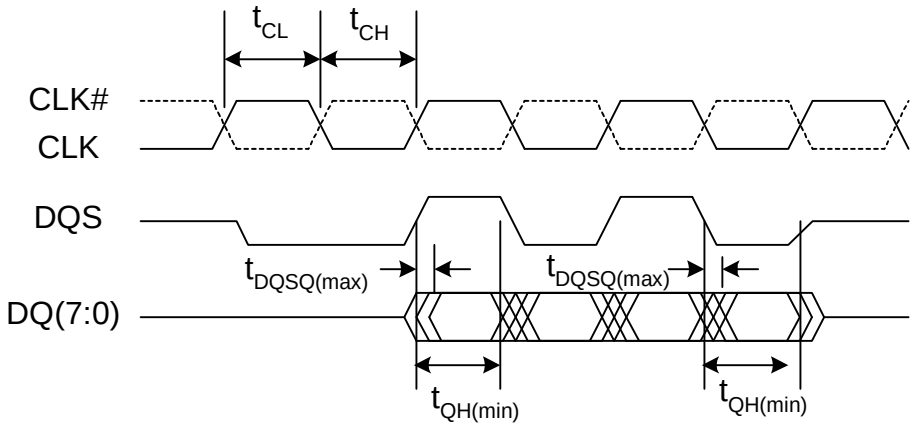


Figure 51: Pulldown slew rate test load

31) For example, a registered DIMM has a t_{HP} of approximately 48% of t_{CK}, calculated as 50% of the period minus both the half period jitter ($t_{JIT(HP)}$) of the PLL and the half period jitter due to crosstalk ($t_{JIT(crosstalk)}$).



t_{DQSQ} and t_{QH} apply for all relevant strobe edges
$t_{HP} = \min(t_{CL}, t_{CH})$
$t_{(CL,CH)} = 0.5 * t_{CK} - t_{JIT(HP)} - t_{JIT(crosstalk)} \geq 0.45 * t_{CK}$

Figure 37 (pg. 61)
DATA OUTPUT (READ) TIMING

32) These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a V_{REF} envelope that has been bandwidth limited to 20MHz.

33) $t_{DAL} = (t_{WR}/t_{CK}$ rounded up + t_{RP}/t_{CK} rounded up) * t_{CK}

34) The high impedance transition of these parameters is not specified to a specific voltage level but specified when the device output begins driving (t_{RPRE}) or is no longer driving (t_{RPST}).

35) The following table specifies derating values for the specifications listed if the single-ended clock slew rate is less than 1.0V/ns

Clk slew rate(Single-ended)	Delta tIH/tIS	Delta tDSS/tDSH	Delta tAC/tDQSCK	Delta tLZ(min)	Delta tHZ(max)
1.0V/ns	0	0	0	0	0
0.75V/ns	+50 ps	+50 ps	+50 ps	-50ps	+50ps
0.5V/ns	+100 ps	+100 ps	+100 ps	-100ps	+100ps

Figure 39a (pg. 63)

POWER-DOWN MODE